Micron Serial NOR Flash Memory Addendum

3V, Multiple I/O, 4KB Sector Erase
N25Q128A13ESFH0E/F

Features

This data sheet addendum provides automotive AC specifications for the N25Q 128Mb, 3V device. The values specified in this addendum replace the same values listed in the general market 128Mb 3V data sheet. This addendum does not provide detailed information of the device. The N25Q 128Mb, 3V general market data sheet should be referenced for a complete description of device functionality, operating modes, and specifications.

- SPI-compatible serial bus interface
- 108 MHz (MAX) clock frequency
- 2.7–3.6V single supply voltage
- Dual/quad I/O instruction provides increased throughput up to 432 MHz
- Supported protocols
  - Extended SPI, dual I/O, and quad I/O
- Execute-in-place (XIP) mode for all three protocols
  - Configurable via volatile or nonvolatile registers
  - Enables memory to work in XIP mode directly after power-on
- PROGRAM/ERASE SUSPEND operations
- Continuous read of entire memory via a single command
  - Fast read
  - Quad or dual output fast read
  - Quad or dual I/O fast read
- Flexible to fit application
  - Configurable number of dummy cycles
  - Output buffer configurable
- Software reset
- 64-byte, user-lockable, one-time programmable (OTP) dedicated area
- Erase capability
  - Subsector erase 4KB uniform granularity blocks
  - Sector erase 64KB uniform granularity blocks
  - Full-chip erase
- Write protection
  - Software write protection applicable to every 64KB sector via volatile lock bit
  - Hardware write protection: protected area size defined by five nonvolatile bits (BP0, BP1, BP2, BP3, and TB)
  - Additional smart protections, available upon request
- Electronic signature
  - JEDEC-standard 2-byte signature (BA18h)
  - Unique ID code (UID): 17 read-only bytes, including:
    - Two additional extended device ID (EDID) bytes to identify device factory options
    - Customized factory data (14 bytes)
- Minimum 100,000 ERASE cycles per sector
- More than 20 years data retention
- Package JEDEC standard, all RoHS compliant
  - SF = SOP2-16 300 mils body width (SO16W)

AC Characteristics and Operating Conditions

The N25Q 128Mb automotive-grade devices support a derating on deselect time (^{t}SHSL1) after a READ command.

Table 1: AC Characteristics and Operating Conditions

Parameter	Symbol	Min	Typ[1]	Max	Unit	Notes
Clock frequency for all commands other than READ (SPI-ER, QIO-SPI protocol)	^{f}C	DC	–	108	MHz	
Clock frequency for READ commands	^{f}R	DC	–	54	MHz	
Clock HIGH time	^{t}CH	4	–	–	ns	2
Clock LOW time	^{t}CL	4	–	–	ns	1
Clock rise time (peak-to-peak)	^{t}CLCH	0.1	–	–	V/ns	3, 4
Clock fall time (peak-to-peak)	^{t}CHCL	0.1	–	–	V/ns	3, 4
S# active setup time (relative to clock)	^{t}SLCH	4	–	–	ns	
S# not active hold time (relative to clock)	^{t}CHSL	4	–	–	ns	
Data in setup time	^{t}DVCH	2	–	–	ns	
Data in hold time	^{t}CHDX	3	–	–	ns	
S# active hold time (relative to clock)	^{t}CHSH	4	–	–	ns	
S# not active setup time (relative to clock)	^{t}SHCH	4	–	–	ns	
S# deselect time after a READ command	^{t}SHSL1	14	–	–	ns	
S# deselect time after a nonREAD command	^{t}SHSL2	50	–	–	ns	
Output disable time	^{t}SHQZ	–	–	8	ns	3
Clock LOW to output valid under 30pF	^{t}CLQV	–	–	7	ns	
Clock LOW to output valid under 10pF		–	–	5	ns	
Output hold time (clock LOW)	^{t}CLQX	1	–	–	ns	
Output hold time (clock HIGH)	^{t}CHQX	1	–	–	ns	
HOLD command setup time (relative to clock)	^{t}HLCH	4	–	–	ns	
HOLD command hold time (relative to clock)	^{t}CHHH	4	–	–	ns	
HOLD command setup time (relative to clock)	^{t}HHCH	4	–	–	ns	
HOLD command hold time (relative to clock)	^{t}CHHL	4	–	–	ns	
HOLD command to output Low-Z	^{t}HHQX	–	–	8	ns	3
HOLD command to output High-Z	^{t}HLQZ	–	–	8	ns	3
Write protect setup time	^{t}WHSL	20	–	–	ns	5
Write protect hold time	^{t}SHWL	100	–	–	ns	5
Enhanced V_{PPH} HIGH to S# LOW for extended and dual I/O page program	^{t}VPPHSL	200	–	–	ns	6
WRITE STATUS REGISTER cycle time	^{t}W	–	1.3	8	ms	
Write NONVOLATILE CONFIGURATION REGISTER cycle time	^{t}WNVCR	–	0.2	3	s	
CLEAR FLAG STATUS REGISTER cycle time	^{t}CFSR	–	40	–	ns	

Table 1: AC Characteristics and Operating Conditions (Continued)

Parameter	Symbol	Min	Typ[1]	Max	Unit	Notes
WRITE VOLATILE CONFIGURATION REGISTER cycle time	tWVCR	–	40	–	ns	
WRITE VOLATILE ENHANCED CONFIGURATION REGISTER cycle time	tWRVECR	–	40	–	ns	
PAGE PROGRAM cycle time (256 bytes)	tPP	–	0.5	5	ms	7
PAGE PROGRAM cycle time (*n* bytes)		–	int(n/8) × 0.015[8]	5	ms	7
PAGE PROGRAM cycle time, $V_{PP} = V_{PPH}$ (256 bytes)		–	0.4	5	ms	7
PROGRAM OTP cycle time (64 bytes)		–	0.2	–	ms	7
Subsector ERASE cycle time	tSSE	–	0.25	0.8	s	
Sector ERASE cycle time	tSE	–	0.7	3	s	
Sector ERASE cycle time (with $V_{PP} = V_{PPH}$)		–	0.6	3	s	
Bulk ERASE cycle time	tBE	–	170	250	s	
Bulk ERASE cycle time (with $V_{PP} = V_{PPH}$)		–	160	250	s	

Notes:
1. Typical values given for T_A = 25 °C.
2. tCH + tCL must add up to 1/fC.
3. Value guaranteed by characterization; not 100% tested.
4. Expressed as a slew-rate.
5. Only applicable as a constraint for a WRITE STATUS REGISTER command when STATUS REGISTER WRITE is set to 1.
6. V_{PPH} should be kept at a valid level until the PROGRAM or ERASE operation has completed and its result (success or failure) is known.
7. When using the PAGE PROGRAM command to program consecutive bytes, optimized timings are obtained with one sequence including all the bytes versus several sequences of only a few bytes (1 < n < 256).
8. int(A) corresponds to the upper integer part of A. For example int(12/8) = 2, int(32/8) = 4 int(15.3) =16.

Revision History

Rev. B – 05/2013

- Changed value of ^{t}SHSL1 from 15 to 14 and added a reference to tSHSL1 in the introductory paragraph

Rev. A – 02/2013

- Initial release

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein.
Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.